PATENT ABSTRACTS OF JAPAN

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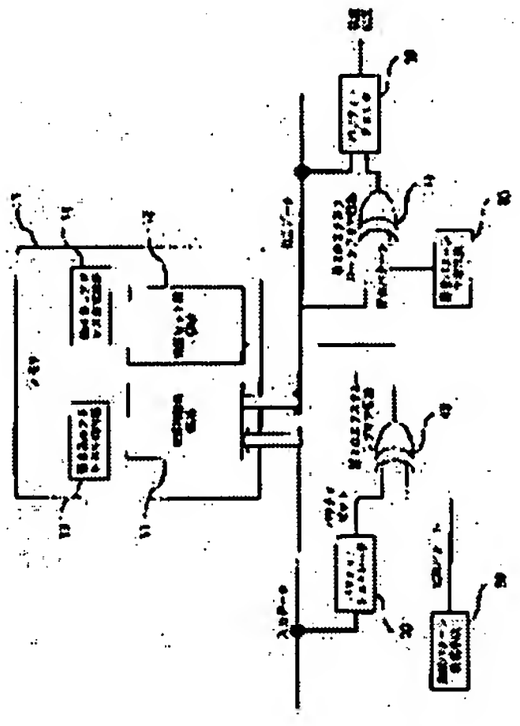
(54) MEMORY MONITORING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To monitor even the fault of wrong storage address in a FIFO memory simultaneously with a parity check without increasing areas for check bits.
SOLUTION: A first exclusive OR circuit 40 exclusively ORs the parity code of data stored in a memory 10 and a monitor pattern related to the storage address inside the memory when writing data to the memory 10. A second exclusive OR circuit 41 exclusively ORs the check bit read out of the memory 10 and a collate pattern related to the storage address in the memory at the time of reading data out of the memory 10. At the time of writing data, the exclusive OR of the parity code of input data and the monitor pattern related to the memory address is written in the memory as the bit for check and at the time of reading data, the exclusive OR of the check bit read out of the memory and the collate pattern related to the memory address is used as the parity bit for performing the parity check.



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CLAIMS

[Claim(s)]
[Claim 1] It has the memory which generates address information, such as FIFO (First In First Out) memory which accumulates the digital signal of a fixed-length packet format temporarily, inside. The field where this memory stores the effective information on data etc., and the field which stores checking information, such as parity, The parity generator which generates the parity bit of the data written in memory, A monitor pattern generation means to generate the monitor pattern depending on the phase in the input data of a fixed-length packet format based on the head information on input data (called a frame pulse and a cel head pulse), The exclusive OR circuit which generates the exclusive OR of said parity bit and said monitor pattern, A collating pattern generation means to generate the pattern which collates the checking information included in the data read from memory based on the head information on output data, The exclusive OR circuit which generates the exclusive OR of said checking information and said collating information, Memory supervisory equipment characterized by making into checking information the exclusive OR of the parity bit about the monitor pattern and data for which have the parity checker who conducts parity check of the data read from memory, and it depends on the phase in the data of a fixed-length packet format.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although the memory supervisory equipment by the conventional parity check method was constituted as mentioned above, there was a trouble of being undetectable, about the failure of a gestalt of mistaking the storing address of memory. Although drawing 5 is the case where the data of a fixed-length packet format are stored to the memory which generates address information like FIFO (First In First Out) memory inside the same integrated circuit, when an invalid data mixes in the interior of memory or failures, such as overwrite of the data to the same address, occur by malfunction of the address information generation circuit inside a FIFO memory, since the relation between effective information and a parity bit is normal, detection of a failure is impossible for it. For example, since it is easy, the case where the data length of input data is 3 bytes is explained. When input data is set with DI#n-j (2 n= 0, 1 and 2, --, j= 1, 3) and a parity bit is set with DIP#n-j (2 n= 0, 1 and 2, --, j= 1, 3), While adding a parity bit to each of these input data, respectively, writing in from Ath [address **] **, and writing in, incrementing the address A write-in address-generation circuit malfunctions and suppose that data **DI#3-1** and **DI#3-2** were written in the discontinuous address. Then, since effective information and a parity bit are still normal conditions when the data written in in the front cycle remain although invalid data will continue from the degree of **DO#3-1** if it reads from Ath [memory address **] ** , and it reads, incrementing the address, in the parity check of data, conflict of judging with it being normal will occur.

[0005] It was not made in order that this invention might solve such a trouble, and it aims at supervising both the failure which mistakes data, and the failure which mistakes the hold address to memory, without increasing a checking bit hold memory area.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to the memory supervisory equipment which supervises the failure of the memory in a digital electronic circuitry.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Drawing 4 is the explanatory view showing actuation of the memory monitor by the parity check method learned widely generally. By this method, it is supervising by adding 1 bit of parity bits in addition to the effective information on data etc., specifying that the sum total of the number of marks becomes odd pieces or even pieces by the writing side, and investigating whether the number of marks by the side of read-out is just like that.
[0003] Next, actuation is explained. The case where it is specified as an example that the number of marks turns into even number is explained. When writing data **DI_A** in address **Ath ** of memory 10, if the number of marks in data ** DI_A** is even and the number of parity generators 20 is **0** and odd, they will make parity bit **DIP_A** **1**. Next, data **DI_A** is written in memory address **Ath ** of the field 11 for effective information, and parity bit **DIP_A** is written in memory address **Ath ** of the field 12 for check bits. when data reading appearance is carried out from Ath [memory address **] **, data **DI_A** and parity bit **DIP_A** are doubled, and if the number of marks is even and the number is normal and odd, it will judge with those with a failure.

[Translation done.]

MEANS

[Means for Solving the Problem] The memory supervisory equipment concerning this invention is equipped with the memory which generates address information, such as a FIFO memory which accumulates the digital signal of a fixed-length packet format temporarily, inside. This memory The field which stores the effective information on data etc., and the field which stores checking information, such as parity, The parity generator which generates the parity bit of the data written in memory, A monitor pattern generation means to generate the monitor pattern depending on the phase in the input data of a fixed-length packet format based on the head information on input data, The exclusive OR circuit which generates the exclusive OR of said parity bit and said monitor pattern, A collating pattern generation means to generate the pattern which collates the checking information included in the data read from memory based on the head information on output data, The exclusive OR circuit which generates the exclusive OR of said checking information and said collating information, It has the parity checker who conducts parity check of the data read from memory, and let the exclusive OR of the parity bit about the monitor pattern and data depending on the phase in the data of a fixed-length packet format be checking information.

[0007]

[Embodiment of the Invention] Gestalt 1. drawing 1 of operation is the block diagram showing the gestalt of 1 operation of the memory supervisory equipment concerning this invention, and explains the actuation in the case of storing the data of a fixed-length packet format in the memory which generates address information like a FIFO memory inside an integrated circuit to coincidence temporarily. In drawing 1 memory and 11 10 The field for effective information storing in memory, The field for checking bit storing in memory and 13 12 The write-in address-generation circuit in memory, The parity generator which generates the parity bit of the data which write 14 in the read-out address-generation circuit in memory, and write 20 in memory, The parity checker who conducts parity check of the data which read 30 from memory, The exclusive OR circuit to which 40 computes the exclusive OR of the output of a monitor pattern and a parity generator 20, The exclusive OR circuit to which 50 computes the exclusive OR of a monitor pattern generation means, and the check bit and collating pattern with which 41 was read from memory, and 60 are collating pattern generation means.

[0008] Next, actuation is explained to be drawing showing the internal state of the memory of drawing 2 based on the timing chart of drawing 3 . Since it is easy, the data length of fixed length data is made into 3 bytes.

If input data DI#n_j (n= 1, 2, --, j= 1, 2, 3) of a fixed-length packet format arrives, input

data is written in from Ath [memory address **] ** of the field 11 for effective information of memory 10, and it writes in, carrying out the increment of the address. Moreover, the monitor pattern generation means 50 generates monitor pattern F#n_j (n= 1, 2, --, j= 1, 2, 3) synchronizing with input data. Although a gestalt changes with systems about generation of a monitor pattern, it is as follows [an outline].
(1) When there is a frame pulse (cel head pulse), share - frame pulse as a monitor pattern. - The pattern, 100, 010, 001, 100, 010, 001, etc., which starts taking advantage of a frame pulse is good anything. [for example,] .
(2) When there is no frame pulse, calculate and judge the head of a frame and generate the same pattern as (1). To coincidence, a parity generator 20 generates parity bit DIP#n_j (n= 1, 2, --, j= 1, 2, 3) about input data. Check bit DIPF#n_j = DIP#n_j~F#n_j which is the exclusive OR of the output of a monitor pattern and a parity generator 20 in the 1st exclusive OR circuit 40 (n= 1, 2, --, j= 1, 2, 3) ---------- (formula 1)
It generates and writes in the field 12 for check bits of memory 10 synchronizing with input data. Here, ~ shows an exclusive OR.
[0009] Being a read-out side, reading from Ath [address **] ** of memory 10 on the other hand, in read-out, and carrying out the increment of the address While reading from the field 11 for effective information of memory 10, reading data DO#n_j (n= 1, 2, --, j= 1, 2, 3) and going Checking information DOPF#n_j (n= 1, 2, --, j= 1, 2, 3) is read from the field 12 for check bits of memory 10. Moreover, the collating pattern generation means 60 generates collating pattern F#n_j (n= 1, 2, --, j= 1, 2, 3) which is the same bit string as a monitor pattern like a monitor pattern generation means. Next, the 2nd exclusive OR circuit 41 generates exclusive-OR DOP#n_j (n= 1, 2, --, j= 1, 2, 3) of said collating pattern and said checking bit. If normal, it is DOPF#n_j = DIPF#n_j (n= 1, 2, --, j= 1, 2, 3). ---------- (formula 2)
Since come out and it is, the output of an exclusive OR circuit 41 is DOP#n_j = DOPF#n_j~F#n_j (n= 1, 2, --, j= 1, 2, 3). ---------- (formula 3)
It becomes. It is DOP#n_j = DIPF#n_j~F#n_j (n= 1, 2, --, j= 1, 2, 3) by substituting (a formula 2) for (a formula 3). ---------- (formula 4)
******. Moreover, it is DOP#n_j = DIP#n_j~F#n_j~F#n_j from (a formula 1). (n= 1, 2, --, j= 1, 2, 3) = DIP#n_j (n= 1, 2, --, j= 1, 2, 3) ---------- (formula 5)
It comes out. Next, output DOP#n_j (n= 1, 2, --, j= 1, 2, 3) of **DO#n_j ** (n= 1, 2, --, j= 1, 2, 3) and an exclusive OR circuit 41 is inputted into the parity checker 30, and parity check is given to him. If normal, it is DO#n_j = DI#n_j (n= 1, 2, --, j= 1, 2, 3). ---------- (formula 6)
It comes out. From (a formula 5) and (a formula 6), since parity check will be conducted about **DI#n_j** and **DIP#n_j ** (n= 1, 2, --, j= 1, 2, 3), the parity checker 30 judges with it being normal.
[0010] For example, the write-in address-generation circuit in memory 10 malfunctions, and suppose that **DI#2-1** and **DI#2-2** were written in the discontinuous address, before writing **DI#2-2** and **DIPF#2-2** in the memory address **A+4th **s. When it reads from Ath [memory address **] **, and the increment of the address is carried out and data are read, after n= 2 and j= 2 Since invalid-data **X** and parity **XP** to it are read, also about the output of an exclusive OR circuit 41 after n= 2 and j= 2 DOP#n_j = DOPF#n_j~F#n_j (n= 2, 3, --, j= 1, 2, 3) = XP~F#n_j (n= 2, 3, --, j= 1, 2, 3) ---------- (formula 7)

It comes out. When it reads from the field 11 for effective information to the parity checker 30 and data DO#n_j (n= 1, 2, --, j= 1, 2, 3) and output DOP#n_j (n= 1, 2, --, j= 1, 2, 3) of an exclusive OR circuit 41 are inputted, therefore, after n= 2 and j= 2 ** Parity check will be conducted about X** and **XP~F#n_j ** (n= 2, 3, --, j= 1, 2, 3). XP Since ~F#n_j (n= 2, 3, --, j= 1, 2, 3) is not usually in agreement with XP, it is judged to be a failure as a result of parity check. Thus, detection of a failure is possible.

[0011] As mentioned above, since not only a parity bit but a monitor pattern is written in memory, it can supervise, without increasing the field for check bits also about the failure from which not only the error of data but the hold address inside memory becomes unusual (with 1 bit).

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, when address information is generated inside memory, it is effective in the ability to supervise both the failure over the hold address of memory, and the failure over data, without increasing the field for check bits (with 1 bit).

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the memory supervisory equipment which supervises the failure of the memory in a digital electronic circuitry.

[0002]

[Description of the Prior Art] Drawing 4 is the explanatory view showing actuation of the memory monitor by the parity check method learned widely generally. By this method, it is supervising by adding 1 bit of parity bits in addition to the effective information on data etc., specifying that the sum total of the number of marks becomes odd pieces or even pieces by the writing side, and investigating whether the number of marks by the side of read-out is just like that.

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[0004]

[Problem(s) to be Solved by the Invention] Although the memory supervisory equipment by the conventional parity check method was constituted as mentioned above, there was a trouble of being undetectable, about the failure of a gestalt of mistaking the storing address of memory. Although drawing 5 is the case where the data of a fixed-length packet format are stored to the memory which generates address information like FIFO (First In First Out) memory inside the same integrated circuit, when an invalid data mixes in the interior of memory or failures, such as overwrite of the data to the same address, occur by malfunction of the address information generation circuit inside a FIFO memory, since the relation between effective information and a parity bit is normal, detection of a failure is impossible for it. For example, since it is easy, the case where the data length of input data is 3 bytes is explained. When input data is set with DI#n-j (2 n= 0, 1 and 2, --, j= 1, 3) and a parity bit is set with DIP#n-j (2 n= 0, 1 and 2, --, j= 1, 3), While adding a parity bit to each of these input data, respectively, writing in from Ath [

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[0011] As mentioned above, since not only a parity bit but a monitor pattern is written in memory, it can supervise, without increasing the field for check bits also about the failure from which not only the error of data but the hold address inside memory becomes unusual (with 1 bit).

[0012]

[Effect of the Invention] According to this invention, when address information is generated inside memory, it is effective in the ability to supervise both the failure over the hold address of memory, and the failure over data, without increasing the field for check bits (with 1 bit).

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the configuration of the gestalt 1 of operation of this invention.

[Drawing 2] It is the explanatory view showing actuation of the gestalt 1 of implementation of this invention.

[Drawing 3] It is the timing chart which shows the flow of actuation of the gestalt 1 of implementation of this invention.

[Drawing 4] It is the block diagram showing the conventional example.

[Drawing 5] It is an explanatory view explaining the technical problem which should be solved.

[Description of Notations]

10 Memory

11 Effective Information Storing Field in Memory

12 Checking Bit Storing Field in Memory

13 Write-in Address-Generation Circuit

14 Read-out Address-Generation Circuit

20 Parity Generator

30 Parity Checker

40 1st Exclusive OR Circuit

41 2nd Exclusive OR Circuit

50 Monitor Pattern Generation Means

60 Collating Pattern Generation Means

[Translation done.]